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EXAMINER	
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ART UNIT	PAPER NUMBER
2841	

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01/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,452	RAPPORT ET AL.	
	Examiner	Art Unit	
	Andargie M. Aychillhum	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/05/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *1-5,7-12,18,26,29 and 32-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,13-28,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

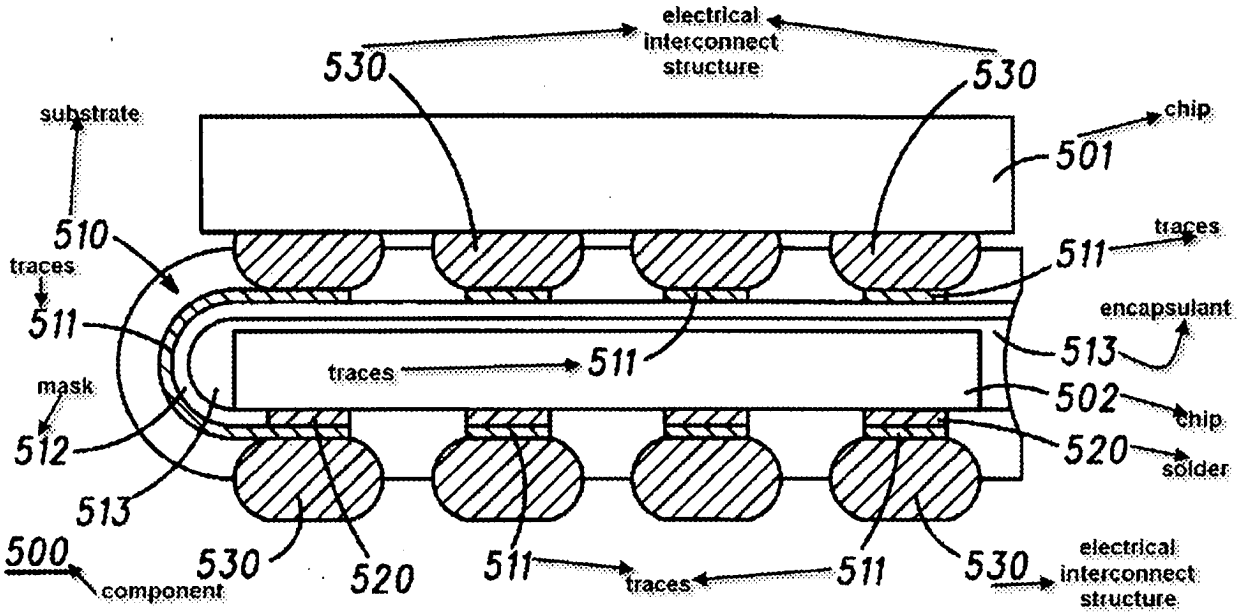
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Mukerji et al. (U.S. 6300679).

As to claim 6, Mukerji discloses in (see fig. **5** below) a high-density circuit module comprising: a first CSP (chip **501**) having an upper and lower major surface (see figure **5** below) and a set of CSP contacts (**530**) along the lower major surface (see figure **5** below); a second CSP (chip **502**) having first and second lateral edges and upper and lower major surfaces (see figure **5** below) and a set of CSP contacts (**520**) along the lower major surface, the first and second lateral edges delineating an extent of the upper major surface of the second CSP (**502**);

A form standard (mask **512**) disposed above the upper surface of the second CSP (**502**); the form standard defining a standard sized form; and

flex circuit (comprising element **510, 511**) that is at least partially disposed about the form standard. (See Mukerji et al. figure 5).



Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 13-31 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Mukerji et al. (US 6,300,679) in views of Karabatsos (US 6,266,252).

Pertaining claim 13, Mukerji et al. discloses a high-density circuit module devised in accordance with claim 6, (see figure above).The first module includes and second integrated circuits (**700, 800,** and **900**) (see Mukerji et al. fig**. 5**).

However, Mukerji et al. does not specifically disclose the memory expansion board; and a switching multiplexer mounted on the memory expansion board, the switching multiplexer for switching data lines; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

Karabatsos discloses the memory expansion board (**10**) (see fig. **1**), and a switching multiplexer (**24**) mounted on the memory expansion board (**10**), the switching multiplexer (**24**) for switching data lines (column **6**, lines **7-21**); and

Decode logic circuit (**26**) for decoding chip (**A or B**), (see fig. **1**) selection signals (column **8**, lines **29-34**) from a control circuit and providing a switching multiplexer (**24**) control signal (column **7**, lines **29-37**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to add a memory expansion board, a switching multiplexer for switching data lines and decode logic circuit as taught by Karabatsos to a high-density circuit disclosed by Mukerji et al. in order to provide a high-speed RAM memory for use in computer systems without sacrificing speed.

Pertaining claim 14, Mukerji et al. as modified by Karabatsos further teaches

a switch (**24** of Karabatsos fig. **1**) for connecting a datapath (column **6**, lines **23-35** of Karabatsos); and

A decode logic (**26** of Karabatsos fig. **1**) for generating a control signal (column **7**, lines **29-37**) that causes the switch (**24**) to connect the data path (column **6**, lines **23-35**) and a combination signal comprised of a clock signal and a chip select signal (column **6**, lines **7-11** of Karabatsos).

Pertaining claim 15, Mukerji et al. discloses a high-density circuit module devised in accordance with claim 6, (see figure above), the high-density circuit module (see figure above), and which plural integrated circuits (**700, 800, 900) (**see Mukerji et al. fig. **5**).

Pertaining claim 16, Mukerji et al. as modified by Karabatsos further teaches the high-density circuit module (see figure above), and which plural integrated circuits (**700, 800, 900)** (see Mukerji et al. of fig. **5**).

A plural memory expansion boards (**10, 12** and **14**) (see Karabatsos fig. 1)

Plural multiplexers (column **6**, lines **23-35**) mounted upon each of the plural memory expansion boards (**10, 12** and **14**), the plural multiplexers for making connections between a datapath (column **6**, lines **23-35**); (see Karabatsos fig. 1) and

Decode logic (**26**) (see Karabatsos fig. 1)on each of the plural memory expansion boards (**10, 12**, and **14)**, the decode logic (**26**) for generating a control signal (column **7**, lines **29-37**) in response to a combination signal comprised of a clock signal and a chip select signal (column **6**, lines **7-11**), the control signal (column **6**, lines **7-11**) causing at least one of the plural multiplexers (column **6**, lines **23-35**) to connect a particular datapath (column **6**, lines **23-35**); (see Karabatsos fig. 1)

Pertaining to claim 17, Mukerji et al. differ from the claimed invention by not showing the multiplexers are FET multiplexers.

Karabatsos teaches the multiplexers (**24**) are FET multiplexers (**field-effect transistor**) (column **6**, lines **23-25**).

Pertaining to claim 19, Mukerji et al. further discloses the plural high-density circuit modules are devised (**700, 800 and 900) (**see Mukerji et al. fig. **5**).

Pertaining to claim 20, Mukerji et al. further discloses the plural high-density circuit modules are devised (**700, 800 and 900) (**see Mukerji et al. of fig**. 5**).

Pertaining to claim 21, Mukerji et al. as modified by Karabatsos further teaches a plurality of integrated circuits **(700, 800, 900) (**see Mukerji et al fig. **5**) and high-density circuit module (see figure above) comprised of first (**700**), second (**800**), third (**900**), and fourth (**500**) individual integrated circuits (see fig. **5-9**).

Karabatsos, from the same field of endeavor as Mukerji et al. discloses memory board (**10**) (see Karabatsos figure **1**) having a board memory signal data (column **8**, lines **29-34**) connection that provides a connection for memory signals between memory control circuitry (column **7**, lines **29-37**);

A switching multiplexer (**24**) (see Karabatsos figure 1) mounted on the memory board (**10**), the switching multiplexer (**24**) (see Karabatsos figure **1**) having a set of plural input data connections (**22 and 24**), (see Karabatsos figure **1**) individual ones of the plural input data connections (**22**) (see Karabatsos figure **1**) connected to provide individual data connections. (Column **6**, lines **22-35**); and

A decode logic circuit (**26**) (see Karabatsos figure **1**) for decoding chip (**A**) selection signals from a control circuit and providing a switching multiplexer control signal (column **7**, lines **29-37**); (see Karabatsos figure **1**).

Pertaining to claim 22, Mukerji et al. differ from the claimed invention by not showing the switching multiplexer further comprises an output data connection connected to the board signal memory data connection.

Karabatsos, from the same field of endeavor as Mukerji et al. discloses the switching multiplexer (**24**) (see fig. **1**), an output data connection connected to the board signal memory data connection (column **3**, lines **32-54**).

Since both Mukerji et al. and Karabatsos teach a dimensional flexible assembly of integrated circuit, method of fabricating the assembly of circuits including a folded flexible substrate with integrated circuit chip, furthermore a method and system for enhancing memory speed and capacity utilizes a set of electronic switches to select a proper termination chip for the computer system bus, it would have been obvious to one having ordinary skill in the art at the time the invention was to have switching multiplexer further comprises an output data connection connected to the board signal memory data connection of Karabatsos in the Mukerji et al. flexible substrate for packaging a semiconductor component in order to provide an high-speed RAM memory for use in computer systems without sacrificing capacity, or alternatively, to provide a high-capacity memory without sacrificing speed and control and timing signals are applied to the control logic and timing generator to provide the necessary control and timing function for the DRAM (a type of random access memory that stores each bit of data in a separate capacitor).

Pertaining to claim 23, Mukerji et al. discloses first (**700**), second (**800**), third (**900**), and fourth (**500**) individual integrated circuits (see fig. **5-9**).

However, Mukerji et al. differ from the claimed invention by not showing the switching multiplexer provides selective individual connection between the board signal memory data connection.

Karabatsos, from the same field of endeavor as Mukerji et al. discloses switching multiplexer (**24**) provides selective individual connection between the board (**10**) signal memory data connection (Column **6**, lines **22-35**).

Since both Mukerji et al. and Karabatsos teach a dimensional flexible assembly of integrated circuit, method of fabricating the assembly of circuits including a folded flexible substrate with integrated circuit chip, furthermore a method and system for enhancing memory speed and capacity utilizes a set of electronic switches to select a proper termination chip for the computer system bus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have switching multiplexer provides selective individual connection between the board signal memory data connection of Karabatsos in the Mukerji et al. flexible substrate for packaging a semiconductor component in order to provide an high-speed RAM memory for use in computer systems without sacrificing capacity, or alternatively, to provide a high-capacity memory without sacrificing speed and control and timing signals are applied to the control logic and timing generator to provide the necessary control and timing function for the DRAM (a type of random access memory that stores each bit of data in a separate capacitor).

Pertaining to claim 24, Mukerji et al. discloses first (**700**), second (**800**), third (**900**), and fourth (**500**) individual integrated circuits (see fig. **5-9**).

However, Mukerji et al. differ from the claimed invention by not showing the individual connection between the board signal memory data connection and in response to the switching multiplexer control signal from the decode logic circuit.

Karabatsos, from the same field of endeavor as Mukerji et al. discloses the board signal memory (**10**) data connection (column **3**, lines **32-54**) and in response to the switching multiplexer (**24**) (see fig. **1**), control signal (column **7**, lines **29-37**); from the decode logic circuit (**26**).

Since both Mukerji et al. and Karabatsos teach a dimensional flexible assembly of integrated circuit, method of fabricating the assembly of circuits including a folded flexible substrate with integrated circuit chip, furthermore a method and system for enhancing memory speed and capacity utilizes a set of electronic switches to select a proper termination chip for the computer system bus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have switching multiplexer further comprises an output data connection connected to the board signal memory data connection of Karabatsos in the Mukerji et al. flexible substrate for packaging a semiconductor component in order to provide an high-speed RAM memory for use in computer systems without sacrificing capacity, or alternatively, to provide a high-capacity memory without sacrificing speed and control and timing signals are applied to the control logic and timing generator to provide the necessary control and

timing function for the DRAM (a type of random access memory that stores each bit of data in a separate capacitor).

Pertaining to claim 25, the teaching of Karabastos includes the decode logic circuit (**26**) is mounted on the memory board (**10**). (See figure **1**).

Pertaining to claim 27, Mukerji et al. as modified by Karabatsos further teaches Y high-density circuit modules **(700)** (see Mukerji et al.) and Z individual integrated circuits **(800)** (see Mukerji et al. fig. **5)**.

X memory expansion boards (**10, 12**, and **14**) (see figure **1** of Karabatso) each populated, the plural multiplexers (24) each for selectively making connections between a datapath. (Column **6**, lines **23-35**);

Decode logic (**26**) on each of the plural memory expansion boards (**10**, **12**, and **14**), the decode logic (**26**) for generating a control signal (column **7**, lines **29-37**) in response to a combination signal comprised of a clock signal (column **7**, lines **29-37**) and chip select signal, the control signal (column **7**, lines **29-37**) causing at least one of the plural multiplexers (column **6**, lines **41-52**) to connect a particular datapath (column **6**, lines **23-35**);

Pertaining to claim 28, Mukerji et al. as modified by Karabatsos further teaches

the multiplexers (**24**) are FET multiplexers (**field-effect transistor**) (column **6**, lines **23-25**). (See Karabatsos figure **1**).

Pertaining to claim 30, Mukerji et al. further discloses the Z equals (**700, 800 and 900) (**see Karabatsos fig**. 5**).

Pertaining to claim 31, Mukerji et al. further discloses the Z equals (**700 and 800). (**See Karabatsos fig**. 5**).

Response to Arguments

5. Applicant's arguments filed 11/05/2007 have been fully considered but they are not persuasive.

Applicant argues "the mask layer 512 of Fig. 5 is a form standard is incorrect. The mask layer of Mukerji is a flexible, electrical insulation layer that is applied over the traces of form directly contacting the semiconductor chip."

In response to the above argument that the form standard as recited in the claim merely the structure below the trace, the prior art shows the structure clearly in fig. 5, therefore, the prior art meets the limitation. it is noted that the claims fail to recite any structure limitation with the regard the form standard defining a standard sized form of the claim that would keep the claims from reading on the interpretation of the reference that the form standard defining a standard sized form reads on (512, figure 5) and flex circuit that is at least partially disposed show on the figure 5.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andargie M. Aychillhum whose telephone number is (571) 270-1607. The examiner can normally be reached on (Mon-Fri from 8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A.A.
January 14th 2008

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